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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. 13435US04)

IN THE APPLICATION OF:

Morteza Cyrus Afghahi, et al.

APPLICATION NO.: 10/795,825

FILED: March 8, 2004

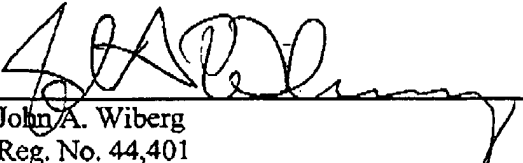
FOR: SINGLE-ENDED SENSE AMPLIFIER
WITH SAMPLE-AND-HOLD
REFERENCE

ART UNIT: 2816

EXAMINER: Kenneth B. Wells

CONF. NO.: 2778

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John A. Wiberg
Reg. No. 44,401

REPLY BRIEF

MS: APPEAL BRIEF-PATENTS

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

Appellant submits this Reply Brief in response to the Examiner's Answer mailed on
December 10, 2010.

Appl. No. 10/795,825
Reply Brief dated February 10, 2011

REMARKS

After reading the Response to Arguments section of the Examiner's Answer, the Appellant has a clearer understanding of the Examiner's arguments and a more thorough understanding of the operation of the circuit shown in FIG. 4A of Kerth, upon which the Examiner's rejection is based. Appellant would thus like to explain why FIG. 4A of Kerth does not anticipate the invention as claimed in claims 9 and 10.

The Examiner asserts that Kerth's operation whereby the voltage at the top input terminal (where VINP is received) is transferred to the left plate of the top capacitor C1, i.e., when the top switch ΦA closes, constitutes the "sampling a voltage present at input node" per claim 9.¹ The Examiner further asserts that the resulting storage of charge on the top capacitor C1 in response to the top switch ΦA , and the other ΦA switch connected to the right plate of top capacitor C1, closing constitutes the "holding the sampled voltage at a reference node as a reference voltage" per claim 9.² Thus, the Examiner deems the "input node" of claim 9 to be the terminal receiving VINP, i.e., the left terminal of top switch ΦA . The Examiner further deems the "reference node" of claim 9 to be the node at the left side of top capacitor C1, and deems the voltage held there at this stage to be the "reference voltage" of claim 9. The Examiner goes on to allege that the operation when the ΦA switches open and the ΦB switches close constitutes the "measuring the input signal at the input node by sampling the input signal and comparing it to the reference voltage" per claim 9.³ Appellant strongly disagrees. Note that when the top switch ΦA is closed, the bottom switch ΦA is also closed.⁴ Therefore, when the ΦA switches are closed and the ΦB switches are open ("subphase 1" per Kerth's terminology), signal VINP is stored at the left terminal of top capacitor C1, and signal VINM is stored at the left terminal of bottom capacitor C1. Note that the Examiner deems the "input node" of claim 9 to be the terminal receiving VINP, and the "reference node" to be the left terminal of top capacitor C1. Then, when the ΦA switches are opened and the ΦB switches are closed ("subphase 2" of Kerth), the signal at the left terminal of top capacitor C1 (which the Examiner deems to be the "reference

¹ Final Office Action, page 3.

² *Id.*

³ *Id.*

⁴ See col. 5, lines 4-6 of Kerth. Also see col. 7, lines 35-39, stating that FIG. 4A operates according to the same principles as FIG. 1A.

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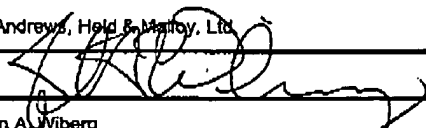
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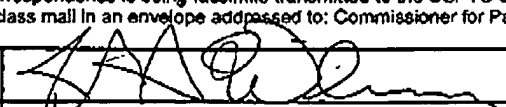
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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10795,825
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	First Named Inventor	Morteza Cyrus Afghani, et al.
	Art Unit	2818
	Examiner Name	Kenneth B. Wells
	Attorney Docket Number	13435US04
Total Number of Pages in This Submission		4

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Firm Name	McAndrews, Held & Malloy, Ltd.		
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Appl. No. 10/795,825

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voltage" of claim 9) is passed to the positive input of amplifier 48. At the same time, the signal at the left terminal of bottom capacitor C1 is passed to the negative input of amplifier 48. Thus the Examiner's "reference voltage" is compared not to "the input signal" received at "the input node" (remember that per the Examiner's rejection, the input signal is signal VINP), but instead to the VINM signal (not surprising since FIG. 4A of Kerth is a differential amplifier, while the method of claim 9 pertains to a single-ended amplifier). Note that in Kerth's subphase 2 (ΦA switches open and ΦB switches closed), the VINP signal is passed to the left terminal of bottom capacitor C1 and stored there, without being passed to the negative input of amplifier 48. This further illustrates that the Examiner's "reference voltage" is not compared to "the input signal" received at "the input node," per claim 9.

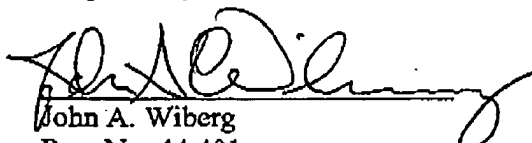
As previously mentioned, Kerth does not explicitly describe the operation of the circuit of FIG. 4A, but instead just states that it operates according to the same principles as FIG. 1A. Col. 5, lines 45-61 of Kerth, describing the operation of the amplifier shown in FIG. 1A, is informative in understanding why the operation of FIG. 4A does not anticipate the method of claim 9.

For at least the foregoing reasons, Appellant submits that claim 9, and claim 10 depending therefrom, are not anticipated by Kerth. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge additional fee(s) or credit overpayment(s) to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Date: February 10, 2011

Respectfully submitted,


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notes/comments:

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John A. Wiberg, Reg. No. 44,401

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